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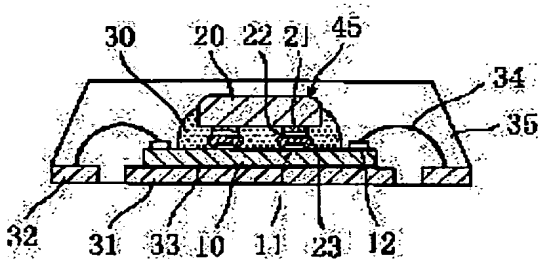
(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress the generation of the package crack of a semiconductor chip on an upper side and the deterioration of the reliability of connection in a semiconductor device for which two semiconductor chips are joined and packaged.
SOLUTION: In this semiconductor device functioning as a three-dimensional device for which two semiconductor chips are joined, the back surface of the semiconductor chip on the upper side is ground, the entire side face of the semiconductor chip on the upper side is covered with a resin layer, or the center of the semiconductor chip on the upper side is made thicker than a peripheral part. Thus, the generation of the package crack is suppressed and the reliability of the semiconductor device is improved.



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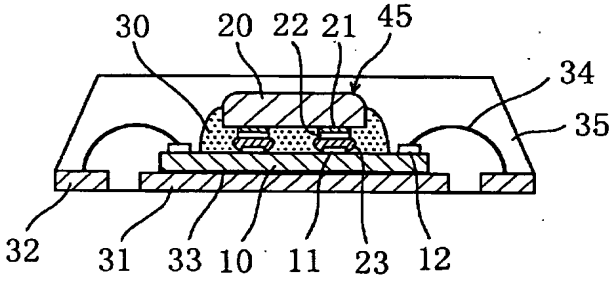
(54)【発明の名称】半導体装置及びその製造方法

(57)【要約】
【課題】　２枚の半導体チップを接合しパッケージ化した半導体装置において、上側の半導体チップのパッケージクラックの発生や接続の信頼性の悪化を抑制する。
【解決手段】　２枚の半導体チップを接合した三次元デバイスとして機能する半導体装置において、上側の半導体チップの裏面を研磨したり、上側の半導体チップの側面全体を樹脂層により覆ったり、あるいは、上側の半導体チップの中央部を周辺部よりも厚くする。これにより、パッケージクラックの発生が抑制され、半導体装置の信頼性が向上する。



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【特許請求の範囲】

【請求項１】　上面に第１の電極を有する第１の半導体チップと、

上面に第２の電極を有し、上記第２の電極を上記第１の電極に電気的に接続させた状態で上記第１の半導体チップ上に搭載された第２の半導体チップとを備え、

上記第２の半導体チップの下面の角部が加工により鈍されていることを特徴とする半導体装置。

【請求項２】　請求項１記載の半導体装置において、

上記第２の半導体チップの下面の角部が曲面となっていることを特徴とする半導体装置。

【請求項３】　請求項２記載の半導体装置において、

上記第２の半導体チップの下面の角部の曲面の曲率半径が１μｍより大きいことを特徴とする請求項１及び請求項２記載の半導体装置。

【請求項４】　請求項１～３のうちいずれか１つに記載の半導体装置において、

上記第１の半導体チップと第２の半導体チップとの間に樹脂層が介在していることを特徴とする半導体装置。

【請求項５】　上面に第１の電極を有する第１の半導体チップと、

上面に第２の電極を有し、上記第２の電極を上記第１の電極に電気的に接続させた状態で上記第１の半導体チップ上に搭載された第２の半導体チップと、

上記第１の半導体チップと第２の半導体チップとの間に介在し、かつ上記第２の半導体チップの全側面を覆う樹脂層とを備えている半導体装置。

【請求項６】　請求項５記載の半導体装置において、

上記樹脂層のうち上記第１の半導体チップと第２の半導体チップとの間に介在する部分と、上記第２の半導体チップの全側面を覆う部分とは、相異なる樹脂材料により構成されていることを特徴とする半導体装置。

【請求項７】　請求項６記載の半導体装置において、

上記樹脂層のうち上記第２の半導体チップの全側面を覆う部分のフィラー含有量は、上記第１の半導体チップと第２の半導体チップとの間に介在する部分のフィラー含有量よりも多いことを特徴とする半導体装置。

【請求項８】　請求項６記載の半導体装置において、

上記樹脂層のうち上記第２の半導体チップの全側面を覆う部分のフィラーの平均径は、上記第１の半導体チップと第２の半導体チップとの間に介在する部分のフィラーの平均径よりも大きいことを特徴とする半導体装置。

【請求項９】　請求項５～８のうちいずれか１つに記載の半導体装置において、

上記樹脂層のうち上記第２の半導体チップの全側面を覆う部分の上面は、上記第２の半導体チップの下面とほぼ共通の平面を有する位置にあることを特徴とする半導体装置。

【請求項１０】　請求項９記載の半導体装置において、

上記第１の半導体チップと上記第２の半導体チップとは、樹脂封止されていることを特徴とする半導体装置。

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【請求項１１】　上面に第１の電極を有する第１の半導体チップと、

上面に第２の電極を有し、上記第２の電極を上記第１の電極に電気的に接続させた状態で上記第１の半導体チップ上に搭載された第２の半導体チップとを備え、

上記第２の半導体チップの中央部は周辺部より厚いことを特徴とする半導体装置。

【請求項１２】　請求項１１記載の半導体装置において、

第１の半導体チップと第２の半導体チップの間に介在する樹脂層をさらに備えていることを特徴とする半導体装置。

【請求項１３】　請求項１２記載の半導体装置において、

上記第１の半導体チップと上記第２の半導体チップとは、樹脂封止されていることを特徴とする半導体装置。

【請求項１４】　第１の半導体チップの上に第２の半導体チップを、両者の電極同士が電気的に互いに接続された状態で搭載してなる半導体装置の製造方法であって、

上面に第１の電極を有し、上記第１の半導体チップになる第１の半導体チップ形成領域を有するウエハと、上面に第２の電極を有する上記第２の半導体チップとを準備する工程と、

上記ウエハの各チップ形成領域の上に、上記第２の半導体チップをそれぞれ搭載して、上記第１の電極と上記第２の電極とを互いに電気的に接続する工程と、

上記ウエハの各チップ形成領域と上記第２の半導体チップとの間に樹脂層を形成する工程と、

上記第２の半導体チップを上記ウエハに搭載した状態で、上記第２の半導体チップの下面を研磨する工程と、

上記ウエハを各チップ形成領域ごとに分離させて、第１の半導体チップの上に第２の半導体チップが搭載されてなる接合体を個別に形成する工程と、

上記第１の半導体チップの上で上記第２の半導体チップを封止樹脂により封止する工程とを含む半導体装置の製造方法。

【請求項１５】　第１の半導体チップの上に第２の半導体チップを、両者の電極同士が電気的に互いに接続された状態で搭載してなる半導体装置の製造方法であって、

上面に第１の電極を有する第１の半導体チップと、上面に第２の電極を有する上記第２の半導体チップとを準備する工程と、

上記第１の半導体チップ形成領域の上に、上記第２の半導体チップを搭載して、上記第１の電極と上記第２の電極とを互いに電気的に接続する工程と、

上記第１の半導体チップと上記第２の半導体チップとの間に樹脂層を形成する工程と、

上記第２の半導体チップを上記ウエハに搭載した状態で、上記第２の半導体チップの下面を研磨する工程と、

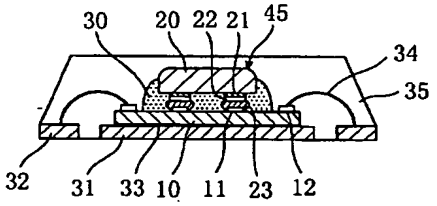
ある。

【図１８】（ａ）～（ｃ）は、従来の三次元デバイスの製造工程を示す断面図である。

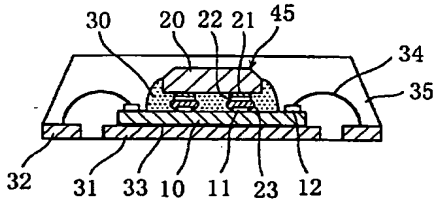
【符号の説明】

１０　第１の半導体チップ
１１　第１の内部電極
１２　ボンディングパッド
２０　第２の半導体チップ
２１　第２の内部電極
２２　バリアメタル層
２３　金属バンプ
３０　樹脂
３１　ダイパッド
３２　リード
３３　導電性ペースト
３４　ボンディングワイヤ
３５　封止樹脂
３６　ウエハ
３７　第１の樹脂層
３８　第２の樹脂層
４０　ツール
４１　紫外線
４２　砥粒
４３　研磨装置
４５　角部
４６　半導体装置
４７　保護樹脂

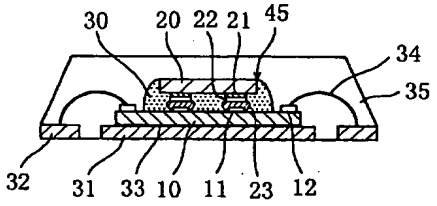
【図１】



【図２】



【図３】



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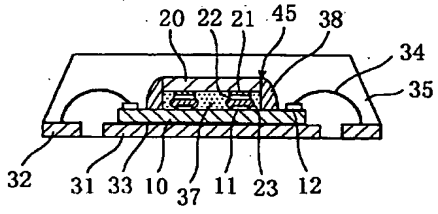

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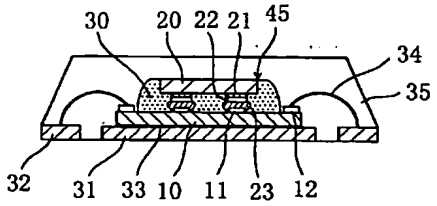

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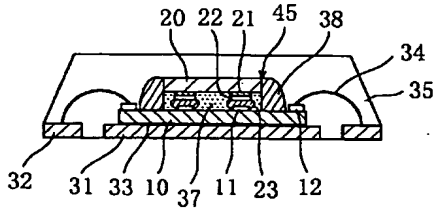
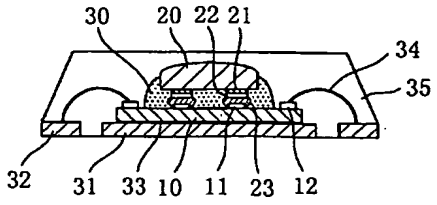


【図７】



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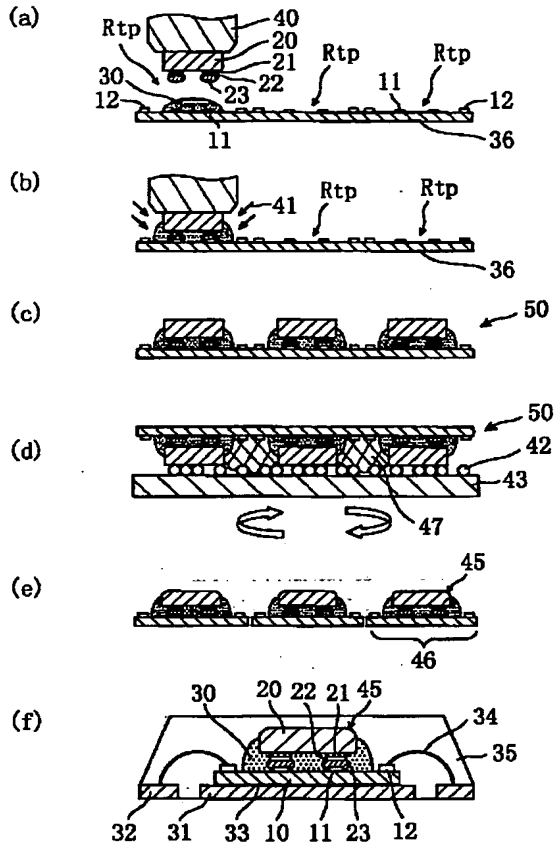

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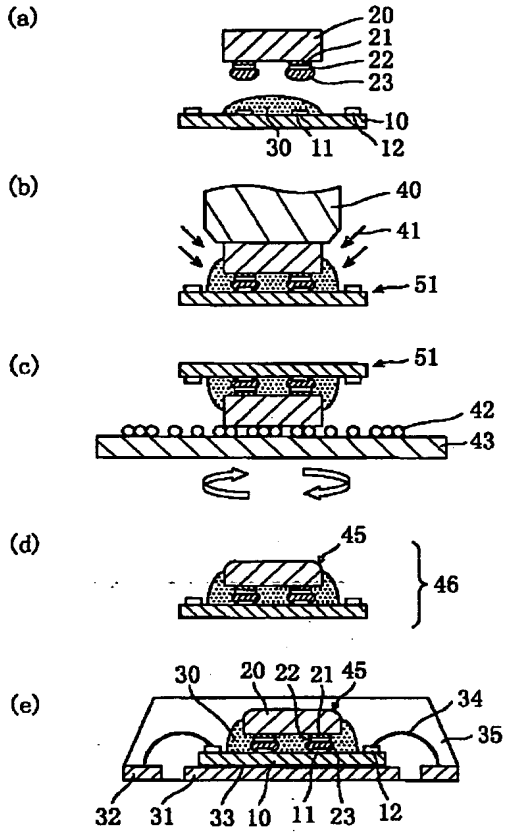
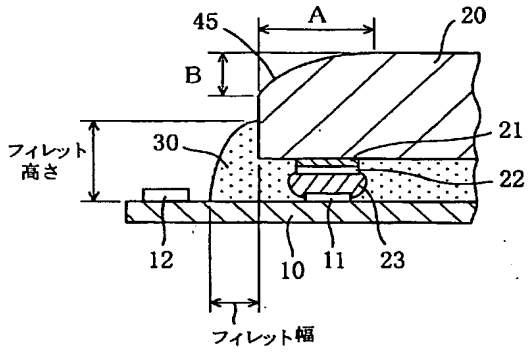
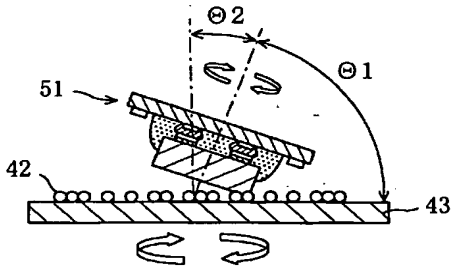


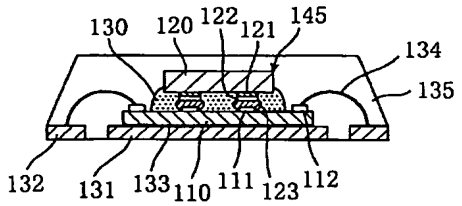
【図１５】



【図１６】



【図１７】



CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by having the 1st semiconductor chip which has the 1st electrode on the top face, and the 2nd semiconductor chip carried on the semiconductor chip of the above 1st where it has the 2nd electrode on the top face and the 2nd electrode of the above is electrically connected to the 1st electrode of the above, and the corner of the underside of the 2nd semiconductor chip of the above becoming dull by processing.

[Claim 2] The semiconductor device characterized by the corner of the underside of the 2nd semiconductor chip of the above serving as a curved surface in a semiconductor device according to claim 1.

[Claim 3] Claim 1 characterized by the radius of curvature of the curved surface of the corner of the underside of the 2nd semiconductor chip of the above being larger than 1 micrometer in a semiconductor device according to claim 2, and a semiconductor device according to claim 2.

[Claim 4] The semiconductor device characterized by the resin layer intervening between the 1st semiconductor chip of the above, and the 2nd semiconductor chip in the semiconductor device of any one publication among claims 1-3.

[Claim 5] The semiconductor device which intervened between the 1st semiconductor chip which has the 1st electrode on the top face, the 2nd

semiconductor chip carried on the semiconductor chip of the above 1st where it has the 2nd electrode on the top face and the 2nd electrode of the above is electrically connected to the 1st electrode of the above, and the 1st semiconductor chip of the above and the 2nd semiconductor chip, and is equipped with the wrap resin layer for all the side faces of the 2nd semiconductor chip of the above.

[Claim 6] It is the semiconductor device characterized by being constituted with the resin ingredient with which a wrap part is different from each other in the part which intervenes between the 1st semiconductor chip of the above, and the 2nd semiconductor chip among the above-mentioned resin layers, and all the side faces of the 2nd semiconductor chip of the above in a semiconductor device according to claim 5.

[Claim 7] It is the semiconductor device characterized by more [among the above-mentioned resin layers] in a semiconductor device according to claim 6 than the filler content of the part to which the filler content of a wrap part intervenes all the side faces of the 2nd semiconductor chip of the above between the 1st semiconductor chip of the above, and the 2nd semiconductor chip.

[Claim 8] It is the semiconductor device characterized by being larger than the pitch diameter of the filler of the part to which the pitch diameter of the filler of a wrap part intervenes all the side faces of the 2nd semiconductor chip of the above between the 1st semiconductor chip of the above, and the 2nd semiconductor chip among the above-mentioned resin layers in a semiconductor device according to claim 6.

[Claim 9] It is the semiconductor device characterized by locating the top face of a wrap part in all the side faces of the 2nd semiconductor chip of the above in the location which has the underside of the 2nd semiconductor chip of the above, and an almost common flat surface among the above-mentioned resin layers in the semiconductor device of any one publication among claims 5-8.

[Claim 10] It is the semiconductor device characterized by carrying out the resin seal of the 1st semiconductor chip of the above, and the 2nd semiconductor chip

of the above in a semiconductor device according to claim 9.
[Claim 11] It is the semiconductor device characterized by having the 1st semiconductor chip which has the 1st electrode on the top face, and the 2nd semiconductor chip carried on the semiconductor chip of the above 1st where it has the 2nd electrode on the top face and the 2nd electrode of the above is electrically connected to the 1st electrode of the above, and the center section of the 2nd semiconductor chip of the above being thicker than a periphery.
[Claim 12] The semiconductor device characterized by having further the resin layer which intervenes between the 1st semiconductor chip and the 2nd semiconductor chip in a semiconductor device according to claim 11.
[Claim 13] It is the semiconductor device characterized by carrying out the resin seal of the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above in a semiconductor device according to claim 12.
[Claim 14] It is the manufacture approach of a semiconductor device that both electrodes come to carry the 2nd semiconductor chip in the condition of having connected mutually electrically on the 1st semiconductor chip. The wafer which has the 1st electrode on the top face and has the 1st semiconductor chip formation field which becomes the 1st semiconductor chip of the above, The process which prepares the 2nd semiconductor chip of the above which has the 2nd electrode for a top face, On each chip formation field of the above-mentioned wafer, the 2nd semiconductor chip of the above is carried, respectively. The process which connects electrically the 1st electrode of the above, and the 2nd electrode of each other of the above, the process which forms a resin layer between each chip formation field of the above-mentioned wafer, and the 2nd semiconductor chip of the above, and where the 2nd semiconductor chip of the above is carried in the above-mentioned wafer The process which grinds the underside of the 2nd semiconductor chip of the above, and the process which forms the zygote with which the above-mentioned wafer is made to separate for every chip formation field, and it comes to carry the 2nd semiconductor chip on the 1st semiconductor chip according to an individual, The manufacture

approach of a semiconductor device including the process which closes the 2nd semiconductor chip of the above with closure resin on the 1st semiconductor chip of the above.

[Claim 15] The 1st semiconductor chip which is the manufacture approach of a semiconductor device that both electrodes come to carry the 2nd semiconductor chip in the condition of having connected mutually electrically on the 1st semiconductor chip, and has the 1st electrode on the top face, The process which prepares the 2nd semiconductor chip of the above which has the 2nd electrode for a top face, The 2nd semiconductor chip of the above is carried on the semiconductor chip formation field of the above 1st. The process which connects electrically the 1st electrode of the above, and the 2nd electrode of each other of the above, the process which forms a resin layer between the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above, and where the 2nd semiconductor chip of the above is carried in the above-mentioned wafer The manufacture approach of a semiconductor device including the process which closes the process which grinds the underside of the 2nd semiconductor chip of the above, and the 1st semiconductor chip of the above and the 2nd semiconductor chip of the above with closure resin.

[Claim 16] The process which connects electrically the 1st electrode of the above and the 2nd electrode of each other of the above in the manufacture approach of a semiconductor device according to claim 14 or 15 is the manufacture approach of the semiconductor device characterized by including further the process which forms a bump in one of electrodes at least among the 1st electrode of the above, and the 2nd electrode of the above, and connects each electrodes through the above-mentioned bump.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device by which the 2nd semiconductor chip was connected on the 1st semiconductor chip, and its manufacturing method.

[0002]

[Description of the Prior Art] In recent years, according to small [of electronic equipment], and processing[high-speed]-izing, the three-dimensions device structure which comes to carry out the laminating of two or more kinds of semiconductor chips is examined widely. When the technique which forms two or more kinds of semiconductor chips into 1 chip according to an individual is compared with the technique which forms a three-dimensions device, there are advantageous and disadvantage according to the class of semiconductor device established in a semiconductor chip. For example, a process becomes complicated and it becomes cost high to form into 1 chip the semiconductor device formed in the mixed-loading process like a memory logic mixed-loading device. Then, by carrying out the laminating of two kinds of semiconductor chips which have the semiconductor device formed of the process suitable according to an individual mutually, the various proposals for using low cost-ization as a drawing wax are made, and there is also a device with which commercial production has started.

[0003] Hereafter, the conventional structure and the conventional manufacture approach of a semiconductor device which were three-dimensions-ized are explained. Drawing 17 is the sectional view showing the structure of the conventional three-dimensions device. Drawing 18 (a) - (c) is the sectional view showing the production process of the above-mentioned conventional three-dimensions device.

[0004] As shown in drawing 17 , the conventional three-dimensions device is equipped with the lead 132 for exchanging an electric signal between the 1st semiconductor chip 110 which has two or more the 1st internal electrodes 111 and bonding pads 112 on the top face, the 2nd semiconductor chip 120 which has two or more 2nd internal electrodes 121 on the top face, the die pad 131 for carrying the 1st semiconductor chip 110 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 110,120, and an external instrument.

[0005] And on the 1st semiconductor chip 110, where alignment of the 1st and 2nd internal electrode 111,121 comrades is carried out, the 2nd semiconductor chip 120 is carried, and the 1st internal electrode 111 and 2nd internal electrode 121 of each other are electrically connected through the metal bump 123. Moreover, it fills up with resin 130 between the 1st semiconductor chip 110 and the 2nd semiconductor chip 120, and the 1st and 2nd semiconductor chip 110,120 pastes up mutually with resin 130, and it is unified. Moreover, the above-mentioned die pad 131 and lead 132 are separated from one leadframe. The 1st semiconductor chip 110 is fixed to a die pad 131 with the golden conductivity pastes 133, such as Pd and Ag, and the bonding pad 112 of the 1st semiconductor chip 110 and the lead 132 are electrically connected through the bonding wire 134. Furthermore, the 1st semiconductor chip 110, the 2nd semiconductor chip 120, a bonding wire 134, a die pad 131, and lead 132 are closed with closure resin 135, and packaging is carried out.

[0006] Next, the manufacture approach of the conventional semiconductor device is explained.

[0007] At the process shown in drawing 18 (a), alignment of the 1st semiconductor chip 110 and 2nd semiconductor chip 120 is carried out with the following procedures. First, the 1st semiconductor chip 110 which has two or more 1st internal electrodes 111 is prepared for a top face, the 1st semiconductor chip 110 is laid on a mounting fixture (not shown), and resin 130 is applied to the top face of the 1st semiconductor chip 110. On the other hand, the 2nd semiconductor chip 120 which has two or more 2nd internal electrodes 121 and the barrier metal 122 on it is prepared for a top face, and the metal bump 123 is formed on the barrier metal 122 of the 2nd semiconductor chip 120. And the 1st semiconductor chip 110 is made to counter above the 1st semiconductor chip 110, where the underside is turned caudad, and alignment of the 1st internal electrode 111 and 2nd internal electrode 121 (barrier metal 122) is carried out.

[0008] Next, the 1st semiconductor chip 110 and 2nd semiconductor chip 120 of each other are joined with the following procedures at the process shown in drawing 18 (b). First, the 1st internal electrode 111 of the 1st semiconductor chip 110 and the internal electrode 121 of the 2nd semiconductor chip 120 are mutually joined through the metal bump 123 who heated and pressurized the 2nd semiconductor chip 120 with the metal tool 140 from the rear face, and was formed on the internal electrode 121 of the 2nd semiconductor chip 120 (on BARIMETARU 122). And resin 130 is stiffened by irradiating ultraviolet rays 141 or heating the resin 130 with which it fills up among both the semiconductor chips 110,120 after junction.

[0009] Next, the following procedures perform a wirebonding process to the semiconductor device joined and unified at the process shown in drawing 18 (c). First, the leadframe 137 which has a die pad 131 and lead 132 is prepared. And the 1st semiconductor chip 110 is fixed with the conductive pastes 133, such as Pd and Ag, on a die pad 131. And the bonding pad 112 of the 1st semiconductor chip 110 and the lead 132 of a leadframe 137 are connected by the bonding wire 134.

[0010] Next, packaging of the semiconductor device which carried out wirebonding is carried out with the following procedures at the process shown in drawing 18 (d). First, the 1st semiconductor chip 110, the 2nd semiconductor chip 120, a bonding wire 134, a die pad 131, and lead 132 are closed by closure resin 135. At this time, the underside or lateral surface of lead 132 is exposed without being covered with closure resin 135, and this part functions as an external terminal.

[0011] The three-dimensions device which carries the 2nd semiconductor chip 120 on the 1st semiconductor chip 110, and it comes to unify according to the above process is formed.

[0012]

[Problem(s) to be Solved by the Invention] However, there were the following nonconformities in the semiconductor device which is the above-mentioned three-dimensions device.

[0013] First, although the 2nd semiconductor chip 120 joined by face down on the 1st semiconductor chip 110 is cut down by dicing from a wafer, the side face of the corner 145 of the underside of the 2nd semiconductor chip 120 is in the condition by which grinding was carried out on the occasion of dicing. Therefore, the stress produced in the case of hardening of closure resin concentrates on the corner 145 of the underside of the 2nd semiconductor chip 120, consequently property degradation of a synthetic semiconductor device becomes easy to take place to it.

[0014] Moreover, also when not closing a semiconductor device by closure resin, it becomes easy for the connection dependability between semiconductor chips to fall under the effect of the curvature of the semiconductor chip at the time of semiconductor device generation of heat.

[0015] The object of this invention is to offer the semiconductor device which eases the stress concentration to the rear-face corner of the 2nd semiconductor chip joined to the 1st semiconductor chip, or can reduce the curvature of a chip, and its manufacture approach.

[0016]

[Means for Solving the Problem] It has the 1st semiconductor chip with which the 1st semiconductor device of this invention has the 1st electrode on the top face, and the 2nd semiconductor chip carried on the semiconductor chip of the above 1st where it has the 2nd electrode on the top face and the 2nd electrode of the above is electrically connected to the 1st electrode of the above, and the corner of the underside of the 2nd semiconductor chip of the above becomes dull by processing.

[0017] Thereby, since the stress concentration to the underside corner of the 2nd semiconductor chip is eased, degradation of the synthetic property of the semiconductor device which is a three-dimensions device -- generating of a package crack etc. is controlled -- is also prevented.

[0018] When the corner of the underside of the 2nd semiconductor chip of the above serves as a curved surface, generating of a package crack is controlled more effectively.

[0019] It is desirable that the radius of curvature of the curved surface of the corner of the underside of the 2nd semiconductor chip of the above is larger than 1 micrometer.

[0020] When the resin layer intervenes between the 1st semiconductor chip of the above, and the 2nd semiconductor chip, the dependability of connection improves.

[0021] The 1st semiconductor chip with which the 2nd semiconductor device of this invention has the 1st electrode on the top face, The 2nd semiconductor chip carried on the semiconductor chip of the above 1st where it has the 2nd electrode on the top face and the 2nd electrode of the above is electrically connected to the 1st electrode of the above, It intervened between the 1st semiconductor chip of the above, and the 2nd semiconductor chip, and has the wrap resin layer for all the side faces of the 2nd semiconductor chip of the above.

[0022] By this, the curvature of a three-dimensions device will be reduced and the dependability of connection will be secured.

[0023] It is more desirable to be constituted by the resin layer in which a wrap part is different from each other in the part which intervenes among the above-mentioned resin layers between the 1st semiconductor chip of the above and the 2nd semiconductor chip of the above, and all the side faces of the 2nd semiconductor chip of the above.

[0024] Or it is more desirable than the filler content of the part to which the filler content of a wrap part intervenes all the side faces of the 2nd semiconductor chip of the above between the 1st semiconductor chip of the above, and the 2nd semiconductor chip among the above-mentioned resin layers that it is larger than the pitch diameter of the filler of the part to which the pitch diameter of the filler of a wrap part intervenes all the side faces of the 2nd semiconductor chip of the above between the 1st semiconductor chip of the above and the 2nd semiconductor chip among the above-mentioned resin layers.

[0025] Since a coefficient of thermal expansion approaches the coefficient of thermal expansion of a semiconductor chip while a modulus of elasticity [in / for all the side faces of the 2nd semiconductor chip / a wrap part] becomes high among resin layers and a chip protection feature improves by the configuration of one of the above, a curvature prevention function also becomes high.

[0026] Among the above-mentioned resin layers, when the top face of a wrap part is located in all the side faces of the 2nd semiconductor chip of the above in the location which has the underside of the 2nd semiconductor chip of the above, and an almost common flat surface, the dependability of connection can be secured more certainly.

[0027] As for the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above, it is desirable that the resin seal is carried out.

[0028] The 3rd semiconductor device of this invention is equipped with the 1st semiconductor chip which has the 1st electrode on the top face, and the 2nd semiconductor chip carried on the semiconductor chip of the above 1st in the state of the face down which it has [down] the 2nd electrode on the top face, and connected the 2nd electrode of the above to the 1st electrode of the above

electrically, and its center section of the 2nd semiconductor chip of the above is thicker than a periphery.

[0029] Thereby, since the curvature of the 2nd semiconductor chip is reduced, the dependability of connection between the 1st semiconductor chip and the 2nd semiconductor chip improves.

[0030] By having further the resin layer which intervenes between the 1st semiconductor chip and the 2nd semiconductor chip, the dependability of connection becomes higher.

[0031] As for the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above, it is desirable that the resin seal is carried out.

[0032] The manufacture approach of the 1st semiconductor device of this invention on the 1st semiconductor chip the 2nd semiconductor chip The wafer which both electrodes are the manufacture approaches of the semiconductor device which it comes to carry in the state of the face down connected mutually electrically, has the 1st electrode on the top face, and has the 1st semiconductor chip formation field which becomes the 1st semiconductor chip of the above, The process which prepares the 2nd semiconductor chip of the above which has the 2nd electrode for a top face, On the 1st semiconductor chip formation field, the 2nd semiconductor chip of the above is carried, respectively. every of the above-mentioned wafer -- The process which connects electrically the 1st electrode of the above, and the 2nd electrode of each other of the above, every of the above-mentioned wafer, where the 2nd semiconductor chip of the above is carried in the above-mentioned wafer, the process which forms a resin layer between the 1st semiconductor chip formation field and the 2nd semiconductor chip of the above, and The process which grinds the underside of the 2nd semiconductor chip of the above, and the process which closes the 2nd semiconductor chip of the above with closure resin on the 1st semiconductor chip of the above are included.

[0033] The semiconductor device by which the stress concentration to a corner was controlled and the package crack was controlled by this approach since the

corner of the underside of the 2nd semiconductor chip was beveled grinding and by being ground is obtained.

[0034] The manufacture approach of the 2nd semiconductor device of this invention on the 1st semiconductor chip the 2nd semiconductor chip The 1st semiconductor chip which both electrodes are the manufacture approaches of the semiconductor device which it comes to carry in the condition of having connected mutually electrically, and has the 1st electrode on the top face, The process which prepares the 2nd semiconductor chip of the above which has the 2nd electrode for a top face, The 2nd semiconductor chip of the above is carried on the semiconductor chip formation field of the above 1st. The process which connects electrically the 1st electrode of the above, and the 2nd electrode of each other of the above, the process which forms a resin layer between the 1st semiconductor chip of the above, and the 2nd semiconductor chip of the above, and where the 2nd semiconductor chip of the above is carried in the above-mentioned wafer The process which grinds the underside of the 2nd semiconductor chip of the above, and the process which forms the zygote with which the above-mentioned wafer is made to separate for every chip formation field, and it comes to carry the 2nd semiconductor chip on the 1st semiconductor chip according to an individual, The process which closes the 1st semiconductor chip of the above and the 2nd semiconductor chip of the above with closure resin is included.

[0035] As for the process which connects electrically the 1st electrode of the above, and the 2nd electrode of each other of the above, in the manufacture approach of the 1st and 2nd semiconductor device of the above, it is desirable to include further the process which forms a bump in one of electrodes at least among the 1st electrode of the above and the 2nd electrode of the above, and connects each electrodes through the above-mentioned bump.

[0036]

[Embodiment of the Invention] (1st operation gestalt) The structure of the semiconductor device concerning the 1st operation gestalt of this invention and

its modification is explained hereafter. Drawing 1 and drawing 2 are the sectional views showing the structure of the three-dimensions device in this operation gestalt and its modification.

[0037] As shown in drawing 1 , the three-dimensions device of this operation gestalt The 1st semiconductor chip 10 which has two or more the 1st internal electrodes 11 and bonding pads 12 in a principal plane, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0038] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. Moreover, it fills up with resin 30 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd semiconductor chip 10 and 20 pastes up mutually with resin 30, and it is unified. Moreover, the above-mentioned die pad 31 and lead 32 are separated from one leadframe. The 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are electrically connected through the bonding wire 34. Furthermore, the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, a die pad 31, and lead 32 are closed with closure resin 35, and packaging is carried out.

[0039] Here, the corner 45 of the rear face of the 2nd semiconductor chip 20 in the three-dimensions device of this operation gestalt is rounded off (curved-surface-ized), and the acute angle corner does not exist in the rear face of ****** and the 2nd semiconductor chip 20. Therefore, the package crack in the corner

45 of the rear face of the 2nd semiconductor chip 20 can be controlled, and degradation of a synthetic device property can be avoided.

[0040] - Modification- drawing 2 is the sectional view of the three-dimensions device in the modification of the 1st operation gestalt. As shown in drawing 2 , in the modification of this operation gestalt, the rear face of the 2nd semiconductor chip 20 is not rounded off, and it bevels at the include angle near 45 degrees. Generating of a package crack etc. can be controlled also by this. That is, the corner 45 of the 2nd semiconductor chip should just become dull.

[0041] (2nd operation gestalt) Drawing 3 is the sectional view showing the structure of the three-dimensions device in this operation gestalt. As shown in this drawing, the three-dimensions device of this operation gestalt The 1st semiconductor chip 10 which has two or more the 1st internal electrode 11 and two or more bonding pads 12 in a principal plane, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0042] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. Moreover, it fills up with resin 30 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd semiconductor chip 10 and 20 pastes up mutually with resin 30, and it is unified. The above-mentioned die pad 31 and lead 32 are separated from one leadframe. The 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are electrically connected through the bonding wire 34. Furthermore, the 1st

semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, a die pad 31, and lead 32 are closed with closure resin 35, and packaging is carried out.

[0043] And in the three-dimensions device of this operation gestalt, the whole side face of the 2nd semiconductor chip 20 is covered with resin 30. Therefore, the corner 45 of the 2nd semiconductor chip 20 will also be protected by this resin 30, the package crack in the corner 45 of the rear face of the 2nd semiconductor chip 20 can be controlled, and degradation of a synthetic device property can be avoided. Moreover, since the 1st semiconductor chip 10 and 2nd semiconductor chip 20 have pasted up strongly with resin 30 before performing a resin seal, peeling of the 1st and 2nd semiconductor chip 10 and 20 in a mounting process can be prevented effectively, and improvement in the dependability of connection can be aimed at.

[0044] - The 1st modification- drawing 4 is the sectional view showing the structure of the semiconductor device in the 1st modification of the 2nd operation gestalt.

[0045] As shown in this drawing, the three-dimensions device in this modification The three-dimensions device shown in drawing 3 , and the 1st semiconductor chip 10 which has two or more the 1st internal electrode 11 and two or more bonding pads 12 in a principal plane similarly, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0046] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. The above-

mentioned die pad 31 and lead 32 are separated from one leadframe. Moreover, the 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are electrically connected through the bonding wire 34.

[0047] Here, in this modification, it fills up with the 1st resin 37 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd semiconductor chip 10 and 20 pastes up mutually with the 1st resin 37, and it is unified. Furthermore, on the 1st semiconductor chip 10, the side face of the 1st resin 37 and the 2nd semiconductor chip 20 is established in the 2nd resin 38 of a wrap.

[0048] And the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, a die pad 31, and lead 32 are closed with closure resin 35, and packaging is carried out.

[0049] Since the whole side face of the 2nd semiconductor chip 20 is covered also with this modification with the 2nd resin 38, the corner 45 of the 2nd semiconductor chip 20 will also be protected by the 2nd resin 38, the package crack in the corner 45 of the rear face of the 2nd semiconductor chip 20 can be controlled, and degradation of a synthetic device property can be avoided according to it. Moreover, since the 1st semiconductor chip 10 and 2nd semiconductor chip 20 have pasted up strongly with resin 37 and 38 before performing a resin seal, peeling of the 1st and 2nd semiconductor chip 10 and 20 in a mounting process can be prevented effectively, and improvement in the dependability of connection can be aimed at.

[0050] And the following effectiveness can be demonstrated by constituting with the resin which has two kinds of the 1st resin 37 and 2nd resin 38 for a resin layer of presentations which are different from each other. For example, there are more filler contents of the 2nd resin 38 than the filler content of the 1st resin 37, or when the pitch diameter of the filler of the 2nd resin 38 is larger than the pitch diameter of the filler of the 1st resin 37, the modulus of elasticity of the 2nd resin

38 becomes high, and the protection feature to the 2nd semiconductor chip 20 corner improves. Moreover, since the coefficient of thermal expansion of the 2nd resin 38 approaches the coefficient of thermal expansion of the 1st and 2nd semiconductor chip 20, a curvature prevention function also becomes high.

[0051] - The 2nd modification- drawing 5 is the sectional view showing the structure of the three-dimensions device in the 2nd modification of the 2nd operation gestalt.

[0052] As shown in this drawing, the three-dimensions device of this operation gestalt The 1st semiconductor chip 10 which has two or more the 1st internal electrode 11 and two or more bonding pads 12 in a principal plane, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0053] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. Moreover, it fills up with resin 30 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd semiconductor chip 10 and 20 pastes up mutually with resin 30, and it is unified. The above-mentioned die pad 31 and lead 32 are separated from one leadframe. The 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are electrically connected through the bonding wire 34. Furthermore, the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, a die pad 31, and lead 32 are closed with closure resin 35, and packaging is carried out.

[0054] And in the three-dimensions device of this operation gestalt, while the whole side face of the 2nd semiconductor chip 20 is covered with resin 30, the upper bed side of resin 30 forms the rear face of the 2nd semiconductor chip 20, and the almost common flat surface. That is, the side of the corner 45 of the rear face of the 2nd semiconductor chip 20 is thickly covered with resin 30. Therefore, the operation effectiveness of protecting the corner 45 of the 2nd semiconductor chip 20 from the structure shown in drawing 3 becomes large.

[0055] - The 3rd modification- drawing 6 is the sectional view showing the structure of the semiconductor device in the 3rd modification of the 2nd operation gestalt. As shown in this drawing, the three-dimensions device in this modification The three-dimensions device shown in drawing 3 , and the 1st semiconductor chip 10 which has two or more the 1st internal electrode 11 and two or more bonding pads 12 in a principal plane similarly, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0056] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. The above-mentioned die pad 31 and lead 32 are separated from one leadframe. Moreover, the 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are electrically connected through the bonding wire 34.

[0057] Here, in this modification, it fills up with the 1st resin 37 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd

semiconductor chip 10 and 20 pastes up mutually with the 1st resin 37, and it is unified. Furthermore, on the 1st semiconductor chip 10, while the side face of the 1st resin 37 and the 2nd semiconductor chip 20 is established in the 2nd resin 38 of a wrap, the upper bed side of the 2nd resin 38 forms the rear face of the 2nd semiconductor chip 20, and the almost common flat surface. That is, the side of the corner 45 of the rear face of the 2nd semiconductor chip 20 is thickly covered with the 2nd resin 38. Therefore, the operation effectiveness of protecting the corner 45 of the 2nd semiconductor chip 20 from the structure shown in drawing 3 becomes large.

[0058] (3rd operation gestalt) Drawing 7 is the sectional view showing the structure of the semiconductor device in the 3rd operation gestalt. As shown in this drawing, the three-dimensions device of this operation gestalt The 1st semiconductor chip 10 which has two or more the 1st internal electrode 11 and two or more bonding pads 12 in a principal plane, The 2nd semiconductor chip 20 which has two or more 2nd internal electrodes 21 in a principal plane, and was joined to the 1st semiconductor chip 10 by the face down, It has the lead 32 for exchanging an electric signal between the die pad 31 for carrying the 1st semiconductor chip 10 of the above, and components, such as a transistor in each above-mentioned semiconductor chip 10 and 20, and an external instrument.

[0059] And on the 1st semiconductor chip 10, where alignment of the 1st and 2nd internal electrode 11 and the 21 comrades is carried out, the 2nd semiconductor chip 20 is carried, and the 1st internal electrode 11 and 2nd internal electrode 21 of each other are electrically connected through the metal bump 23. Moreover, it fills up with resin 30 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the 1st and 2nd semiconductor chip 10 and 20 pastes up mutually with resin 30, and it is unified. The above-mentioned die pad 31 and lead 32 are separated from one leadframe. The 1st semiconductor chip 10 is fixed to a die pad 31 with the golden conductivity pastes 33, such as Pd and Ag, and the bonding pad 12 of the 1st semiconductor chip 10 and the lead 32 are

electrically connected through the bonding wire 34. Furthermore, the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, a die pad 31, and lead 32 are closed with closure resin 35, and packaging is carried out.

[0060] Here, as for the 2nd semiconductor chip 20, in the three-dimensions device of this operation gestalt, the center section has become thicker than a periphery. Therefore, according to the three-dimensions device of this operation gestalt, the package crack of the 2nd semiconductor chip 20 can be controlled, and degradation of a synthetic device property can be avoided.

[0061] In addition, in the three-dimensions device of this operation gestalt, although only the lower part of the side face of the 2nd semiconductor chip 20 is covered with resin 30 and the whole side face of the 2nd semiconductor chip 20 is not covered with resin 30, the whole side face of the 2nd semiconductor chip 20 shall be covered with resin 30 like the 2nd operation gestalt.

[0062] (4th operation gestalt) Next, the manufacture approach of the semiconductor device concerning the 4th operation gestalt of this invention is explained. In this operation gestalt, the manufacture approach of the semiconductor device concerning the 1st above-mentioned operation gestalt is explained. Drawing 8 (a) - (f) is the sectional view showing the production process of the semiconductor device in this operation gestalt.

[0063] Alignment of the wafer 36 and the 2nd semiconductor chip 20 which have the chip formation field Rtp of a large number which are the fields for forming the 1st semiconductor chip 10 with the following procedures at the process shown in drawing 8 (a) is carried out. First, the wafer 36 which has many chip formation fields Rtp is prepared. A semiconductor device and wiring are formed in each chip formation field Rtp of a wafer 36, and two or more bonding pads 12 which consist of two or more the 1st internal electrodes 11 and aluminum which consist of aluminum are formed in the top face of each chip formation field Rtp. And a wafer 36 is laid on a mounting fixture (not shown), and the resin 30 constituted by the top face of one chip formation field Rtp of a wafer 36 with epoxy etc. is

applied. As resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen from a chip size etc. Moreover, not only spreading to the chip formation field Rtp of a wafer 36 but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0064] Moreover, ****** [the timing] after it carries out alignment of the timing which applies resin 30 not only in before the alignment shown in drawing 8 (a) and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 8 (b)).

[0065] The 2nd semiconductor chip 20 which, on the other hand, has two or more 2nd internal electrodes 21 which become a principal plane from aluminum, and the barrier metal layer 22 on it is prepared, and the metal bump 23 is formed on the barrier metal layer 22 of the 2nd semiconductor chip 20. The barrier metal layer 22 consists of a metal thin film of Ti, Cu, and nickel, and the metal bump 23 consists of Sn-Pb. It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0066] And the 2nd semiconductor chip 20 is made to counter one chip formation field Rtp of a wafer 36, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 with a tool 40 above one chip formation field Rtp of a wafer 36.

[0067] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, a metal bump may be formed like the 2nd internal electrode 21 of the 2nd semiconductor chip 20 on the 1st internal electrode 11 on the chip formation field Rtp of a wafer 36.
 [0068] Next, the chip formation field Rtp and the 2nd semiconductor chip 20 of a wafer

36 are mutually joined with the following procedures at the process shown in drawing 8 (b).

[0069] First, it is made to descend, holding the 2nd semiconductor chip 20 with a tool 40, and alignment of the metal bump 23 who formed on the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and the 1st internal electrode 11 arranged to one chip formation field Rtp of a wafer 36 is performed. And heating and application of pressure of the 1st internal electrode 11 on the wafer 36 by which alignment was carried out, and the metal bump 23 of the 2nd semiconductor chip 20 are done using a tool 40, and it joins using a physical operation or a metal study-operation (operation of the alloying by atomic counter diffusion etc.). When it applies before joining resin 30 (at process shown in drawing 8 (a)), in case a tool 40 is dropped and junction of each internal electrode 11 and 12 comrades is performed, resin 30 can extend between the chip formation field Rtp of a wafer 36, and the 2nd semiconductor chip 20. At this time, the temporary fixed force between the 2nd semiconductor chip 20 and a wafer 36 increases further according to the viscosity of resin 30. Although an about [0.1-20g] load is suitable about one metal bump 23, the welding pressure by the tool 40 sets up the magnitude of this load so that constraint of the 1st internal electrode 11 being damaged or not changing the property of semiconductor devices, such as a transistor currently formed in that 1st internal electrode 11 bottom, wiring, etc. may be filled. Then, resin 30 is stiffened and the 2nd semiconductor chip 20 and wafer 36 are made to unify. In that case, if resin 30 is a photo-setting resin, ultraviolet rays 41 will be heated, respectively, if it is thermosetting resin. When hardening the resin 30 by heating, the heater which performed heating by heater implements, such as oven, after discharge of the application of pressure by the tool 40, or was made to build in a tool 40 performs direct heating at the time of application of pressure. Although the temperature conditions at the time of heat curing are based also on the construction material of resin 30, about 70-300 degrees C is required for them.

[0070] Next, the structure of a zygote 50 where carry many 2nd semiconductor

chip 20 on a wafer 36, and only the number of the 2nd semiconductor chips 20 which carry the process shown in drawing 8 (a) and (b) in each chip formation field Rtp of a wafer 36 becomes by ****** at the process shown in drawing 8 (c) repeatedly as shown in drawing 8 (c) is acquired. In addition, it is also possible to substitute the anisotropy electric conduction film ACF (Anisotropic Conductor Film) which contains Au, nickel, Ag, etc. as an electric conduction particle including an epoxy resin, acrylic resin, etc. as a resinous principle, or anisotropy electric conduction resin ACP (Anisotropic Conductor Paste) for the resin 30 with which it is filled up between semiconductor chip-wafers.

[0071] Next, the rear face of the 2nd semiconductor chip 20 in a zygote 50 is ground at the process shown in drawing 8 (d). After fully stiffening resin 30 at the process shown in drawing 8 (c), a zygote 50 is laid on polish equipment 43 in the condition of having made the rear face (field it has turned [field] to the upper part) of the 2nd semiconductor chip 20 carried on each chip formation field Rtp of a wafer 36 countering the top face of polish equipment 43. At this time, protection resin 47 is formed on the field between each chip field Rtp of a wafer 36. And the rear face of each 2nd semiconductor chip 20 is ground by rotating polish equipment 43, supplying the polish abrasive grain 42 to the polished surface of polish equipment 43, and adding a load to a zygote 50. At this time, as a polish abrasive grain 42, the diamond abrasive grain whose grain size is about #1200-#2000 is desirable, and the rotational frequency of polish equipment 43 has desirable 5 - 50rpm extent.

[0072] Next, if polish is ended and a zygote 50 is removed from polish equipment 43 at the process shown in drawing 8 (e), the configuration by which the corner 45 of the rear face of each 2nd semiconductor chip 20 on a wafer 36 was curved-surface-ized by becoming blunt will be acquired. In addition, the dimension a of the chip longitudinal direction shown in drawing 15 is about 1-10 micrometers, and the configuration of the corner 45 of the rear face of the 2nd semiconductor chip 20 is a configuration from which the dimension B of a chip lengthwise direction is set to about 1-10 micrometers. Then, the semiconductor device 46

which consists of each the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is obtained by carrying out the dicing of the wafer 36 for every chip formation field Rtp of a zygote 50.

[0073] Next, packaging of a semiconductor device 46 is performed at the process shown in drawing 8 (f). First, both are fixed with the conductive paste 33 which carries a semiconductor device 46 in the die pad 31 of a leadframe, and contains Pd, Ag, etc. And the lead 32 of a leadframe is connected with the bonding pad 12 of the 1st semiconductor chip 10 by the bonding wire 34 which consists of Au of 25 micrometerphi extent, aluminum, etc. And finally, the closure resin 35 of an epoxy system or a polyimide system is used for the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, the die pad 31 of a leadframe, and the lead 32 (part) of a leadframe, and a resin seal is performed.

[0074] The three-dimensions device of the 1st operation gestalt which carries the 2nd semiconductor chip 20 on the 1st semiconductor chip 10, and it comes to unify according to the above process is formed easily.

[0075] - Explain the manufacture approach of the semiconductor device concerning the modification of modification -, next the 4th operation gestalt. Drawing 9 (a) - (e) is the sectional view showing the production process of the semiconductor device in the modification of the 4th operation gestalt. In this modification, after carrying out the dicing of the wafer and already forming the 1st semiconductor chip 10, the 2nd semiconductor chip 20 is joined on the 1st semiconductor chip 10.

[0076] Therefore, at the process shown in drawing 9 (a), alignment of the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is carried out. The conditions at this time are easy to be as having explained in drawing 8 (a) except the conditions described below. Moreover, as resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen

from a chip size etc. Moreover, not only spreading to the wafer 36 with which the 1st semiconductor chip 10 has been arranged but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0077] Moreover, ****** [the timing] after it carries out alignment of the timing which applies resin 30 not only in before the alignment shown in drawing 9 (a) and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 9 (b)).

[0078] It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient formed on the 2nd semiconductor chip 20, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0079] And the 2nd semiconductor chip 20 is made it to counter the 1st semiconductor chip 10, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 above the 1st semiconductor chip 10 with a tool 40.

[0080] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, it may replace with the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and a metal bump may be formed on the 1st internal electrode 11 of the 1st semiconductor chip 10.

[0081] Next, with the same procedure as the process shown in already explained drawing 8 (b) at the process shown in drawing 9 (b), the 2nd semiconductor chip 20 is carried in the 1st semiconductor chip 10, junction of both internal electrode 11 and 21 comrades and hardening of resin 30 are performed, and the zygote 51 which comes to carry the 2nd semiconductor chip 20 on the 1st semiconductor chip 10 is formed.

[0082] Next, the same procedure as the process shown in drawing 9 (c) drawing 8 [which was already explained] (d) - (f) at the process shown in - (e) performs the 2nd polish process, wirebonding process, packaging process, etc. of a semiconductor chip 20 on the back of a zygote 51.

[0083] In this modification, since supply of the abrasive grain 42 to the corner 45

of the rear face of the 2nd semiconductor chip 20 is more smoothly performed by [which are the processes shown in drawing 9 (c), and comes to join the 1st and 2nd semiconductor chip 10 and 20] grinding the rear face of the 2nd semiconductor chip 20 every zygote 51, easy-ization of polish can be attained compared with the approach of the 4th operation gestalt.

[0084] (5th operation gestalt) Next, the manufacture approach of the semiconductor device concerning the 5th operation gestalt of this invention is explained. In this operation gestalt, the manufacture approach of the semiconductor device concerning the 2nd above-mentioned operation gestalt is explained. Drawing 10 (a) - (f) is the sectional view showing the production process of the semiconductor device in this operation gestalt.

[0085] Alignment of the wafer 36 and the 2nd semiconductor chip 20 which have the chip formation field Rtp of a large number which are the fields for forming the 1st semiconductor chip 10 with the following procedures at the process shown in drawing 10 (a) is carried out. First, the wafer 36 which has many chip formation fields Rtp is prepared. A semiconductor device and wiring are formed in each chip formation field Rtp of a wafer 36, and two or more bonding pads 12 which consist of two or more the 1st internal electrodes 11 and aluminum which consist of aluminum are formed in the top face of each chip formation field Rtp. And a wafer 36 is laid on a mounting fixture (not shown), and the resin 30 constituted by the top face of one chip formation field Rtp of a wafer 36 with epoxy etc. is applied. As resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen from a chip size etc. Moreover, not only spreading to the chip formation field Rtp of a wafer 36 but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0086] Moreover, ****** [the timing] after it carries out alignment of the timing which applies resin 30 not only in before the alignment shown in drawing 10 (a)

and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 10 (b)).

[0087] Here, in this operation gestalt, although it changes with conditions, such as area of the 2nd semiconductor chip 20, especially, the conditions by the class of semiconductor chip and the amount which can form the fillet of resin in the side face of the 2nd semiconductor chip 20 are required for the amount of the resin 30 applied. Concretely, as for the amount of resin 30, it is desirable that it is the amount set to (refer to drawing 15) and about 50-300 micrometers or more by the fillet height or fillet width of face of resin 30 after hardening.

[0088] The 2nd semiconductor chip 20 which, on the other hand, has two or more 2nd internal electrodes 21 which become a principal plane from aluminum, and the barrier metal layer 22 on it is prepared, and the metal bump 23 is formed on the barrier metal layer 22 of the 2nd semiconductor chip 20. The barrier metal layer 22 consists of a metal thin film of Ti, Cu, and nickel, and the metal bump 23 consists of Sn-Pb. It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0089] And the 2nd semiconductor chip 20 is made to counter one chip formation field Rtp of a wafer 36, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 with a tool 40 above one chip formation field Rtp of a wafer 36.

[0090] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, it may replace with the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and a metal bump may be formed on the 1st internal electrode 11 on the chip formation field Rtp of a wafer 36.

[0091] Next, the chip formation field Rtp and the 2nd semiconductor chip 20 of a wafer 36 are mutually joined with the following procedures at the process shown

in drawing 10 (b).

[0092] First, it is made to descend, holding the 2nd semiconductor chip 20 with a tool 40, and alignment of the metal bump 23 who formed on the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and the 1st internal electrode 11 arranged to one chip formation field Rtp of a wafer 36 is performed. And heating and application of pressure of the 1st internal electrode 11 on the wafer 36 by which alignment was carried out, and the metal bump 23 of the 2nd semiconductor chip 20 are done using a tool 40, and it joins using a physical operation or a metal study-operation (operation of the alloying by atomic counter diffusion etc.). When it applies before joining resin 30 (at process shown in drawing 10 (a)), in case a tool 40 is dropped and junction of each internal electrode 11 and 12 comrades is performed, resin 30 can extend between the chip formation field Rtp of a wafer 36, and the 2nd semiconductor chip 20. At this time, the temporary fixed force between the 2nd semiconductor chip 20 and a wafer 36 increases further according to the viscosity of resin 30. Although an about [0.1-20g] load is suitable about one metal bump 23, the welding pressure by the tool 40 sets up the magnitude of this load so that constraint of the 1st internal electrode 11 being damaged or not changing the property of semiconductor devices, such as a transistor currently formed in that 1st internal electrode 11 bottom, wiring, etc. may be filled. Then, resin 30 is stiffened and the 2nd semiconductor chip 20 and wafer 36 are made to unify. In that case, if resin 30 is a photo-setting resin, ultraviolet rays 41 will be heated, respectively, if it is thermosetting resin. When hardening the resin 30 by heating, the heater which performed heating by heater implements, such as oven, after discharge of the application of pressure by the tool 40, or was made to build in a tool 40 performs direct heating at the time of application of pressure. Although the temperature conditions at the time of heat curing are based also on the construction material of resin 30, about 70-300 degrees C is required for them.

[0093] Next, the structure of a zygote 50 where carry many 2nd semiconductor chip 20 on a wafer 36, and only the number of the 2nd semiconductor chips 20

which carry the process shown in drawing 10 (a) and (b) in each chip formation field Rtp of a wafer 36 becomes by ****** at the process shown in drawing 10 (c) repeatedly as shown in drawing 10 (c) is acquired. In addition, it is also possible to substitute the anisotropy electric conduction film ACF, anisotropy electric conduction resin ACP, etc. for the resin 30 with which it is filled up between semiconductor chip-wafers.

[0094] Next, the rear face of the 2nd semiconductor chip 20 in a zygote 50 is ground at the process shown in drawing 10 (d). After fully stiffening resin 30 at the process shown in drawing 1010 (c), a zygote 50 is laid on polish equipment 43 in the condition of having made the rear face (field it has turned [field] to the upper part) of the 2nd semiconductor chip 20 carried on each chip formation field Rtp of a wafer 36 countering the top face of polish equipment 43. At this time, protection resin 47 is formed on the field between each chip furnace machine Rtp of a wafer 36. And the rear face of each 2nd semiconductor chip 20 is ground by rotating polish equipment 43, supplying the polish abrasive grain 42 to the polished surface of polish equipment 43, and adding a load to a zygote 50. At this time, as a polish abrasive grain 42, the diamond abrasive grain whose grain size is about #1200-#2000 is desirable, and the rotational frequency of polish equipment 43 has desirable 5 - 50rpm extent.

[0095] Here, in this operation gestalt, the rear face of the 2nd semiconductor chip 20 is ground until the upper bed section of the part which is on the side face of the 3rd semiconductor chip 20 among resin 30 is exposed.

[0096] Next, if polish is ended and a zygote 50 is removed from polish equipment 43 at the process shown in drawing 10 (e), the configuration with which the whole side face of each 2nd semiconductor chip 20 on a wafer 36 is covered with resin 30 will be acquired.

[0097] Then, the semiconductor device 46 which consists of each the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is obtained by carrying out the dicing of the wafer 36 for every chip formation field Rtp of a zygote 50.

[0098] Next, packaging of a semiconductor device 46 is performed at the process

shown in drawing 10 (f). First, both are fixed with the conductive paste 33 which carries a semiconductor device 46 in the die pad 31 of a leadframe, and contains Pd, Ag, etc. And the lead 32 of a leadframe is connected with the bonding pad 12 of the 1st semiconductor chip 10 by the bonding wire 34 which consists of Au of 25 micrometerphi extent, aluminum, etc. And finally, the closure resin 35 of an epoxy system or a polyimide system is used for the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, the die pad 31 of a leadframe, and the lead 32 (part) of a leadframe, and a resin seal is performed.

[0099] The three-dimensions device of the 2nd operation gestalt which carries the 2nd semiconductor chip 20 on the 1st semiconductor chip 10, and it comes to unify according to the above process is formed easily.

[0100] - Explain the manufacture approach of the semiconductor device concerning the 1st modification of 1st modification -, next the 5th operation gestalt. Drawing 11 (a) - (e) is the sectional view showing the production process of the semiconductor device in the 1st modification of the 5th operation gestalt. In this modification, after carrying out the dicing of the wafer and already forming the 1st semiconductor chip 10, the 2nd semiconductor chip 20 is joined on the 1st semiconductor chip 10.

[0101] Therefore, at the process shown in drawing 11 (a), alignment of the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is carried out. The conditions at this time are easy to be as having explained in drawing 10 (a) except the conditions described below. Moreover, as resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen from a chip size etc. Moreover, not only spreading to the wafer 36 with which the 1st semiconductor chip 10 has been arranged but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0102] Moreover, ****** [the timing] after it carries out alignment of the timing

which applies resin 30 not only in before the alignment shown in drawing 11 (a) and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 11 (b)).

[0103] It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient formed on the 2nd semiconductor chip 20, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0104] And the 2nd semiconductor chip 20 is made it to counter the 1st semiconductor chip 10, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 above the 1st semiconductor chip 10 with a tool 40.

[0105] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, it may replace with the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and a metal bump may be formed on the 1st internal electrode 11 of the 1st semiconductor chip 10.

[0106] Next, with the same procedure as the process shown in already explained drawing 10 (b) at the process shown in drawing 11 (b), the 2nd semiconductor chip 20 is carried in the 1st semiconductor chip 10, junction of both internal electrode 11 and 21 comrades and hardening of resin 30 are performed, and the zygote 51 which comes to carry the 2nd semiconductor chip 20 on the 1st semiconductor chip 10 is formed.

[0107] Next, the same procedure as the process shown in drawing 11 (c) drawing 10 [which was already explained] (d) - (f) at the process shown in - (e) performs the 2nd polish process, wirebonding process, packaging process, etc. of a semiconductor chip 20 on the back of a zygote 51.

[0108] In this modification, it is the process shown in drawing 11 (c), and easy-ization of polish can be attained compared with the approach of the 5th operation gestalt by [which come to join the 1st and 2nd semiconductor chip 10 and 20] grinding the rear face of the 2nd semiconductor chip 20 every zygote 51.

[0109] - Explain the manufacture approach of the semiconductor device

concerning the 2nd modification of 2nd modification -, next the 5th operation gestalt of this invention. In this modification, the three-dimensions device in the 2nd modification of the 2nd operation gestalt is formed. Drawing 12 (a) - (f) is the sectional view showing the production process of the semiconductor device in the 2nd modification of the 5th operation gestalt.

[0110] The process and basic target which show the formation procedure of the three-dimensions device in this modification to drawing 10 (a) - (f) in the operation gestalt of the above 5th are the same.

[0111] Here, in this modification, it is the process shown in drawing 12 (d), and after the upper bed section of the part which is on the side face of the 2nd semiconductor chip 20 among resin 30 is exposed, the 2nd semiconductor chip 20 and resin 30 are ground further. The three-dimensions device which has a configuration in which the rear face of the 2nd semiconductor chip 20 and the upper bed side of resin 30 form the almost common flat surface 45 by this polish approach is formed.

[0112] In this modification, it is the process shown in drawing 12 (c), and easy-ization of polish can be attained compared with the approach of the 5th operation gestalt by [which come to join the 1st and 2nd semiconductor chip 10 and 20] grinding the rear face of the 2nd semiconductor chip 20 every zygote 51.

[0113] - Explain the manufacture approach of the semiconductor device concerning the 3rd modification of 3rd modification -, next the 5th operation gestalt of this invention. Also in this modification, the manufacture approach of the semiconductor device in the 2nd modification of the 2nd operation gestalt is explained. Drawing 13 (a) - (e) is the sectional view showing the production process of the semiconductor device in the 3rd modification of the 5th operation gestalt. In this modification, after carrying out the dicing of the wafer and already forming the 1st semiconductor chip 10, the 2nd semiconductor chip 20 is joined on the 1st semiconductor chip 10.

[0114] Therefore, at the process shown in drawing 13 (a), alignment of the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is carried out. The

conditions at this time are easy to be as having explained in drawing 10 (a) except the conditions described below. Moreover, as resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen from a chip size etc. Moreover, not only spreading to the wafer 36 with which the 1st semiconductor chip 10 has been arranged but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0115] Moreover, ****** [the timing] after it carries out alignment of the timing which applies resin 30 not only in before the alignment shown in drawing 13 (a) and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 13 (b)).

[0116] It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient formed on the 2nd semiconductor chip 20, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0117] And the 2nd semiconductor chip 20 is made it to counter the 1st semiconductor chip 10, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 above the 1st semiconductor chip 10 with a tool 40.

[0118] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, it may replace with the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and a metal bump may be formed on the 1st internal electrode 11 of the 1st semiconductor chip 10.

[0119] Next, with the same procedure as the process shown in already explained drawing 10 (b) at the process shown in drawing 13 (b), the 2nd semiconductor chip 20 is carried in the 1st semiconductor chip 10, junction of both internal electrode 11 and 21 comrades and hardening of resin 30 are performed, and the zygote 51 which comes to carry the 2nd semiconductor chip 20 on the 1st

semiconductor chip 10 is formed.

[0120] Next, the same procedure as the process shown in drawing 13 (c) drawing 10 [which was already explained] (d) - (f) at the process shown in - (e) performs the 2nd polish process, wirebonding process, packaging process, etc. of a semiconductor chip 20 on the back of a zygote 51.

[0121] In this modification, it is the process shown in drawing 13 (c), and easy-ization of polish can be attained compared with the approach of the 2nd modification by [which come to join the 1st and 2nd semiconductor chip 10 and 20] grinding the rear face of the 2nd semiconductor chip 20 every zygote 51.

[0122] (6th operation gestalt) Next, the manufacture approach of the semiconductor device concerning the 6th operation gestalt of this invention is explained. In this operation gestalt, the manufacture approach of the semiconductor device concerning the 3rd above-mentioned operation gestalt is explained. Drawing 14 (a) - (f) is the sectional view showing the production process of the semiconductor device in this operation gestalt.

[0123] At the process shown in drawing 14 (a), alignment of the 1st semiconductor chip 10 and 2nd semiconductor chip 20 is carried out with the following procedures. First, the wafer which has many chip formation fields in which a semiconductor device and wiring were formed is prepared. And a wafer is cut down for every chip formation field by dicing, and the 1st semiconductor chip 10 is formed. Two or more bonding pads 12 which consist of two or more the 1st internal electrodes 11 and aluminum which consist of aluminum are formed in the top face of the 1st semiconductor chip 10. And the 1st semiconductor chip 10 is laid on a mounting fixture (not shown), and the resin 30 constituted by the top face of the 1st semiconductor chip 10 with epoxy etc. is applied. As resin 30, there are the thermosetting and room-temperature-setting nature other than epoxy, and there are acrylic resin, polyimide resin, urethane resin, etc. as a resin ingredient. Moreover, as the method of application of resin, there is the dispensing method, print processes, or the **********ing method, and a suitable approach is chosen from a chip size etc. Moreover, not only

spreading to the 1st semiconductor chip 10 but spreading of resin can be replaced with spreading to the 2nd semiconductor chip 20.

[0124] Moreover, ****** [the timing] after it carries out alignment of the timing which applies resin 30 not only in before the alignment shown in drawing 14 (a) and it joins each internal electrode 11 and 21 comrades through the metal bump 23 (process shown in drawing 14 (b)).

[0125] Here, in this operation gestalt, although it changes with conditions, such as area of the 2nd semiconductor chip 20, especially, the conditions by the class of semiconductor chip and the amount which can form the fillet of resin in the side face of the 2nd semiconductor chip 20 are required for the amount of the resin 30 applied. Concretely, the amount of resin 30 is the fillet height or fillet width of face (refer to drawing 15) of resin 30 after hardening, and it is desirable that it is an amount used as about 50-300 micrometers or more.

[0126] The 2nd semiconductor chip 20 which, on the other hand, has two or more 2nd internal electrodes 21 which become a principal plane from aluminum, and the barrier metal layer 22 on it is prepared, and the metal bump 23 is formed on the barrier metal layer 22 of the 2nd semiconductor chip 20. The barrier metal layer 22 consists of a metal thin film of Ti, Cu, and nickel, and the metal bump 23 consists of Sn-Pb. It is possible to choose and use any one of Au, In, In-Sn, Sn-Ag, Sn-Cu, Sn-Zn, and Cu(s) and nickel as the metal bump's 23 ingredient, and the diameter of a bump is [3-100 micrometers and the height of this metal bump's 23 size] 3-50 micrometers.

[0127] And the 2nd semiconductor chip 20 is made it to counter the 1st semiconductor chip 10, where the rear face is turned caudad, holding the 2nd semiconductor chip 20 above the 1st semiconductor chip 10 with a tool 40.

[0128] In addition, as a member for performing electrical installation, a conductive paste besides the metal bump 23, anisotropy electric conduction resin, metal filler distribution resin, etc. can be used. Moreover, it may replace with the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and a metal bump may be formed on the 1st internal electrode 11 of the 1st semiconductor chip 10.

[0129] Next, the 1st semiconductor chip 10 and 2nd semiconductor chip 20 of each other are joined with the following procedures at the process shown in drawing 14 (b).

[0130] First, it is made to descend, holding the 2nd semiconductor chip 20 with a tool 40, and alignment of the metal bump 23 who formed on the 2nd internal electrode 21 of the 2nd semiconductor chip 20, and the 1st internal electrode 11 arranged at the 1st semiconductor chip 10 is performed. And heating and application of pressure of the 1st internal electrode 11 on the 1st semiconductor chip 10 by which alignment was carried out, and the metal bump 23 of the 2nd semiconductor chip 20 are done using a tool 40, and it joins using a physical operation or a metal study-operation (operation of the alloying by atomic counter diffusion etc.). When it applies before joining resin 30 (at process shown in drawing 10 (a)), in case a tool 40 is dropped and junction of each internal electrode 11 and 12 comrades is performed, resin 30 can extend between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20. At this time, the temporary fixed force between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20 increases further according to the viscosity of resin 30. Although an about [0.1-20g] load is suitable about one metal bump 23, the welding pressure by the tool 40 sets up the magnitude of this load so that constraint of the 1st internal electrode 11 of the 1st semiconductor chip 10 being damaged, or not changing the property of semiconductor devices, such as a transistor currently formed in that 1st internal electrode 11 bottom, wiring, etc. may be filled. Then, resin 30 is stiffened and the 1st semiconductor chip 10 and 2nd semiconductor chip 20 are made to unify. In that case, if resin 30 is a photo-setting resin, ultraviolet rays 41 will be heated, if it is thermosetting resin. When hardening the resin 30 by heating, the heater which performed heating by heater implements, such as oven, after discharge of the application of pressure by the tool 40, or was made to build in a tool 40 performs direct heating at the time of application of pressure. Although the temperature conditions at the time of heat curing are based also on the construction material of resin 30, about 70-300

degrees C is required for them.

[0131] By the above processing, the structure of a zygote 51 of coming to carry the 2nd semiconductor chip 20 on the 1st semiconductor chip 10 is acquired. In addition, it is also possible to substitute the anisotropy electric conduction film ACF, anisotropy electric conduction resin ACP, etc. for the resin 30 with which it is filled up between semiconductor chip-wafers.

[0132] Next, the rear face of the 2nd semiconductor chip 20 in a zygote 50 is ground at the process shown in drawing 14 (d). After fully stiffening resin 30 at the process shown in drawing 1414 (c), a zygote 51 is laid on polish equipment 43 in the condition of having made the rear face (field it has turned [field] to the upper part) of the 2nd semiconductor chip 20 carried on the 1st semiconductor chip 10 countering the top face of polish equipment 43. And the rear face of each 2nd semiconductor chip 20 is ground by rotating polish equipment 43, supplying the polish abrasive grain 42 to the polished surface of polish equipment 43, and adding a load to a zygote 51. At this time, as a polish abrasive grain 42, the diamond abrasive grain whose grain size is about #1200-#2000 is desirable, and the rotational frequency of polish equipment 43 has desirable 5 - 50rpm extent.

[0133] Here, in this operation gestalt, it grinds by rotating a zygote 51 and polish equipment 43, changing the angle of inclination theta 2 over the normal of the polished surface of the polish equipment 43 of a zygote 51, as shown in drawing 15 . Thereby, after termination of a polish process, as shown in drawing 14 (a), while continuing and rounding off the corner 45 of the rear face of the 2nd semiconductor chip 20 in the larger range, the semiconductor device 46 formed so that the center section of the 2nd semiconductor chip 20 might become thicker than a periphery can be obtained.

[0134] Next, packaging of a semiconductor device 46 is performed at the process shown in drawing 14 (f). First, a semiconductor device 46 is carried in the die pad 31 of a leadframe, and both are fixed with the conductive paste 33 containing Pd, Ag, etc. And the lead 32 of a leadframe is connected with the bonding pad 12 of the 1st semiconductor chip 10 by the bonding wire 34 which consists of Au of 25

micrometerphi extent, aluminum, etc. And finally, the closure resin 35 of an epoxy system or a polyimide system is used for the 1st semiconductor chip 10, the 2nd semiconductor chip 20, a bonding wire 34, the die pad 31 of a leadframe, and the lead 32 (part) of a leadframe, and a resin seal is performed.

[0135] The three-dimensions device of the 3rd operation gestalt which carries the 2nd semiconductor chip 20 on the 1st semiconductor chip 10, and it comes to unify according to the above process is formed easily.

[0136] In addition, in the 3rd operation gestalt, the structure shown in the modification of the 1st operation gestalt shown in drawing 2 can be easily acquired by seting constant the angle of inclination theta 2 over the normal of the polish grinding stone side of a zygote 51, and performing grinding in the condition which shows in above-mentioned drawing 16 R> 6, using the grinding attachment which has a polish grinding stone instead of polish equipment 43.

[0137] in addition, above-mentioned the 4- as shown in drawing 4 or drawing 6 , the 2nd resin 38 of a wrap is applied and you may make it stiffen the 1st resin 37 made to intervene between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the side face of the 2nd semiconductor chip 20 according to an individual in the 6th operation gestalt

[0138] In addition, in each above-mentioned operation gestalt, although the field in which the 1st and 2nd internal electrode 11 and 21 is formed was made into the principal plane of the 1st and 2nd semiconductor chip 10 and 20, this invention is not limited to this operation gestalt. therefore, the conductor prepared in the through hole and side face of a semiconductor chip about the 1st semiconductor chip 10 or 2nd semiconductor chip 20 -- this invention is applicable through the film also about what prepared the internal electrode in the rear face of a semiconductor chip.

[0139]

[Effect of the Invention] According to the semiconductor device or its manufacture approach of this invention, generating of a package crack, lowering of the connection dependability between each semiconductor chip, etc. can be

controlled by making the corner of the underside of the 2nd semiconductor chip joined to the 1st semiconductor chip curved-surface-ize, and making the center section of a bonnet or the 2nd semiconductor chip thicker than a periphery for the whole side face of the 2nd semiconductor chip by the resin layer.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the three-dimensions device in the 1st operation gestalt of this invention.
[Drawing 2] It is the sectional view of the three-dimensions device in the modification of the 1st operation gestalt of this invention.
[Drawing 3] It is the sectional view of the three-dimensions device in the 2nd operation gestalt of this invention.
[Drawing 4] It is the sectional view of the semiconductor device in the 1st modification of the 2nd operation gestalt.
[Drawing 5] It is the sectional view of the semiconductor device in the 2nd modification of the 2nd operation gestalt.
[Drawing 6] It is the sectional view of the semiconductor device in the 3rd

modification of the 2nd operation gestalt.

[Drawing 7] It is the sectional view of the three-dimensions device in the 3rd operation gestalt of this invention.

[Drawing 8] (a) - (f) is the sectional view showing the production process of the semiconductor device in the 4th operation gestalt.

[Drawing 9] (a) - (e) is the sectional view showing the production process of the semiconductor device in the modification of the 4th operation gestalt.

[Drawing 10] (a) - (f) is the sectional view showing the production process of the semiconductor device in the 5th operation gestalt.

[Drawing 11] (a) - (e) is the sectional view showing the production process of the semiconductor device in the 1st modification of the 5th operation gestalt.

[Drawing 12] (a) - (f) is the sectional view showing the production process of the semiconductor device in the 2nd modification of the 5th operation gestalt.

[Drawing 13] (a) - (e) is the sectional view showing the production process of the semiconductor device in the 3rd modification of the 5th operation gestalt.

[Drawing 14] (a) - (f) is the sectional view showing the production process of the semiconductor device in the 6th operation gestalt.

[Drawing 15] It is the sectional view showing the corner of the rear face of the 2nd semiconductor chip in the 1st operation gestalt of this invention in a detail.

[Drawing 16] It is the sectional view showing the polish approach of the rear face of the 2nd semiconductor chip in the 6th operation gestalt of this invention.

[Drawing 17] It is the sectional view showing the structure of the conventional three-dimensions device.

[Drawing 18] (a) - (c) is the sectional view showing the production process of the conventional three-dimensions device.

[Description of Notations]

10 1st Semiconductor Chip

11 1st Internal Electrode

12 Bonding Pad

20 2nd Semiconductor Chip

21 2nd Internal Electrode

22 Barrier Metal Layer

23 Metal Bump

30 Resin

31 Die Pad

32 Lead

33 Conductive Paste

34 Bonding Wire

35 Closure Resin

36 Wafer

37 1st Resin Layer

38 2nd Resin Layer

40 Tool

41 Ultraviolet Rays

42 Abrasive Grain

43 Polish Equipment

45 Corner

46 Semiconductor Device

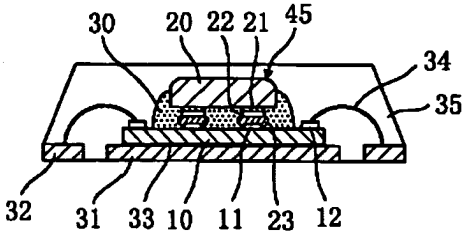
47 Protection Resin

[Translation done.]

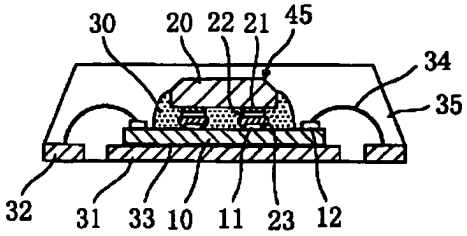
* NOTICES *

DRAWINGS

[Drawing 1]



[Drawing 2]



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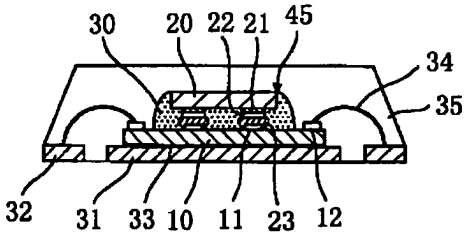

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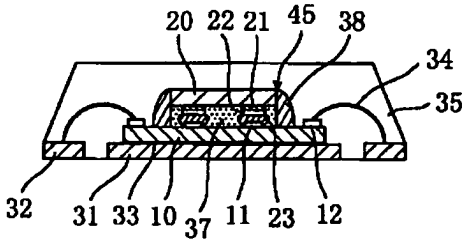

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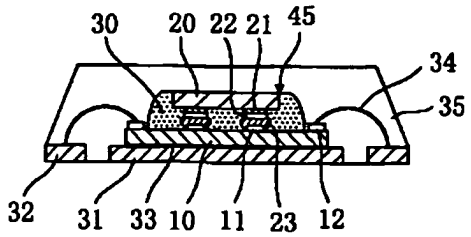

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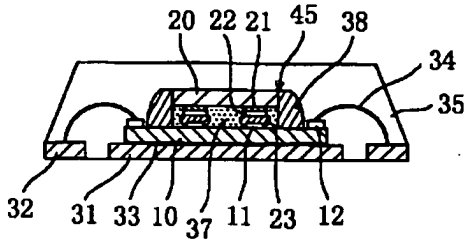

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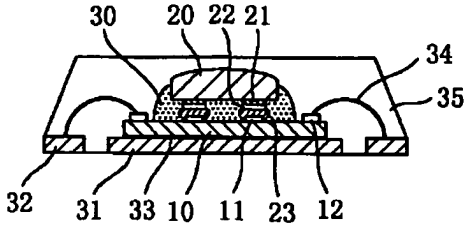

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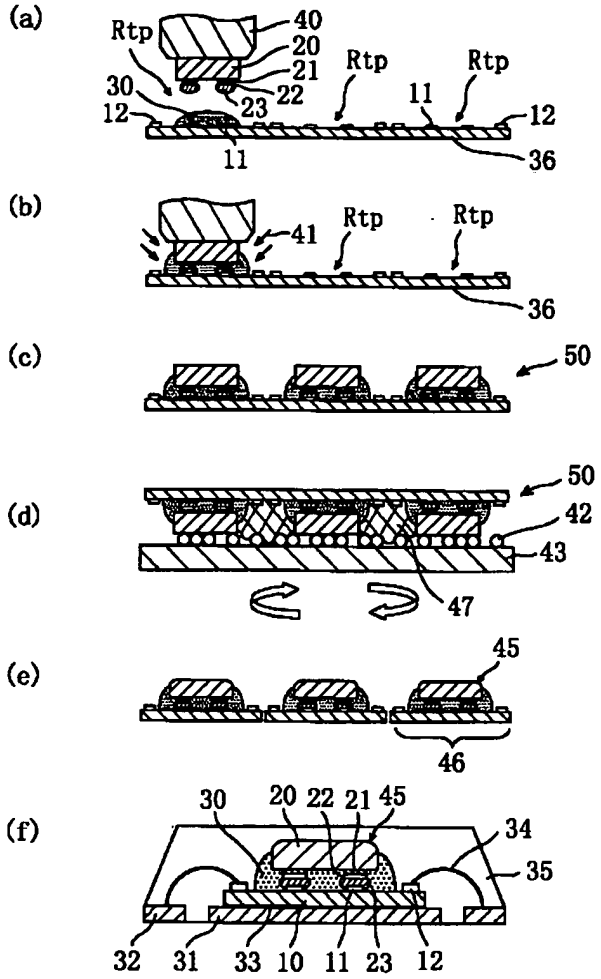
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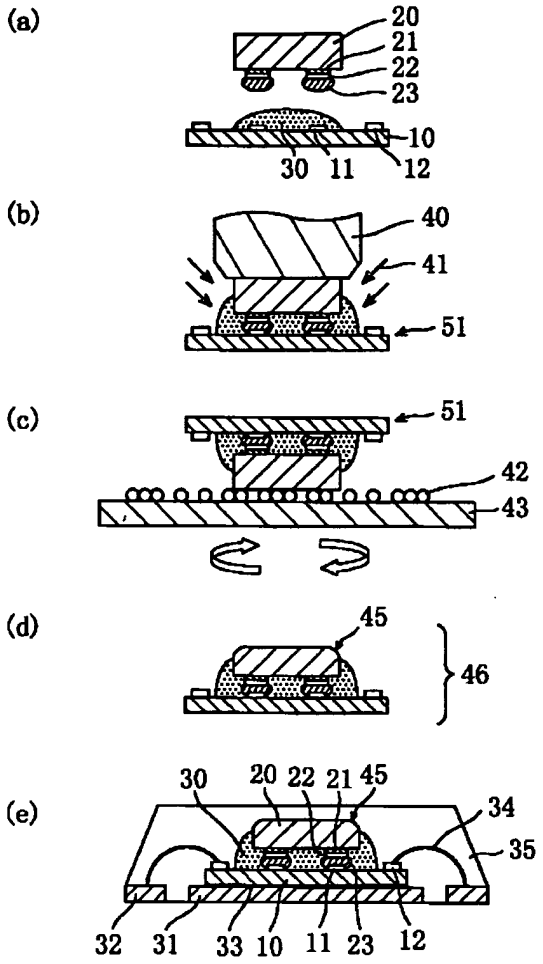
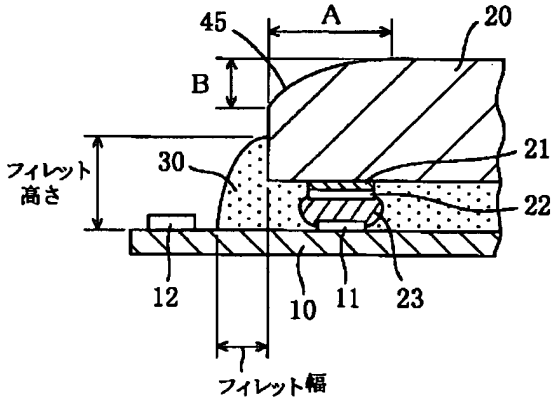
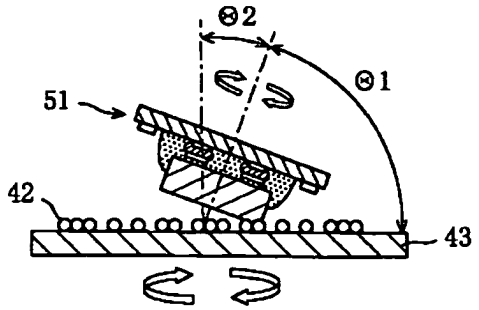
[Drawing 9]



[Drawing 15]



[Drawing 16]



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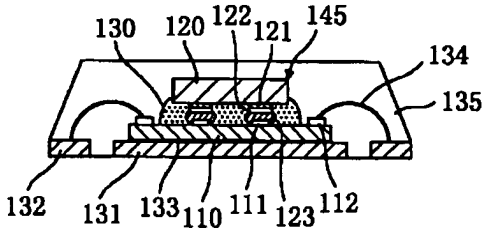


[Drawing 10]

(a)

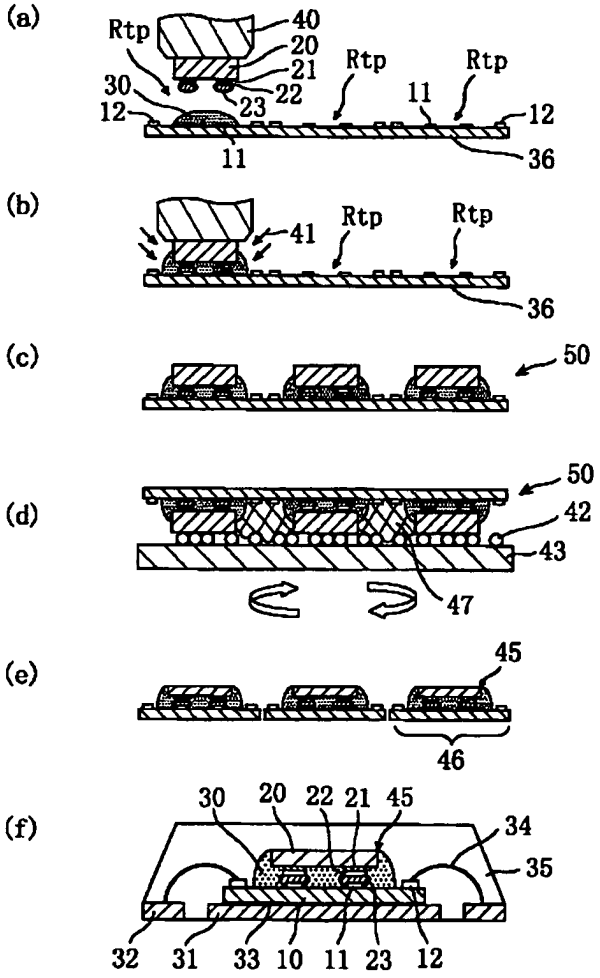
(b)

(c)

(d)

(e)

(f)



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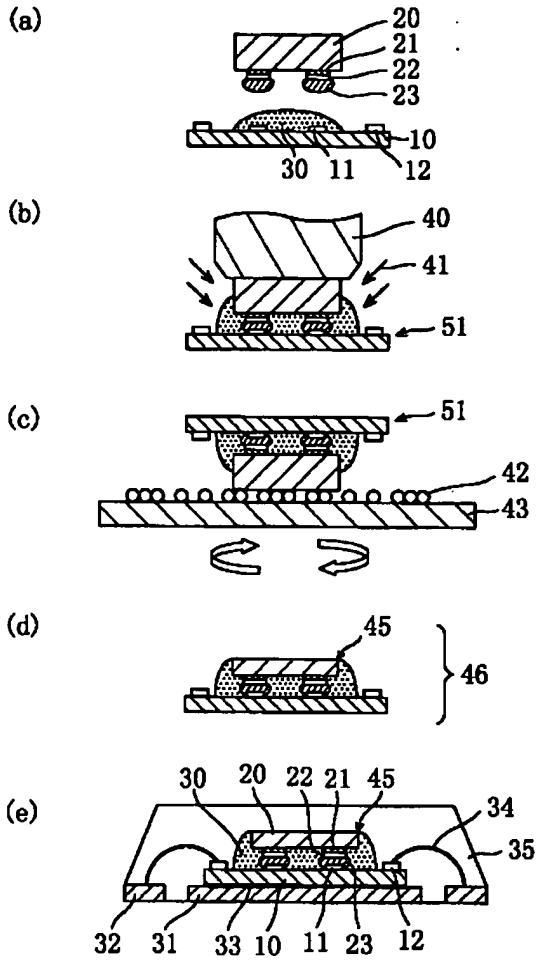

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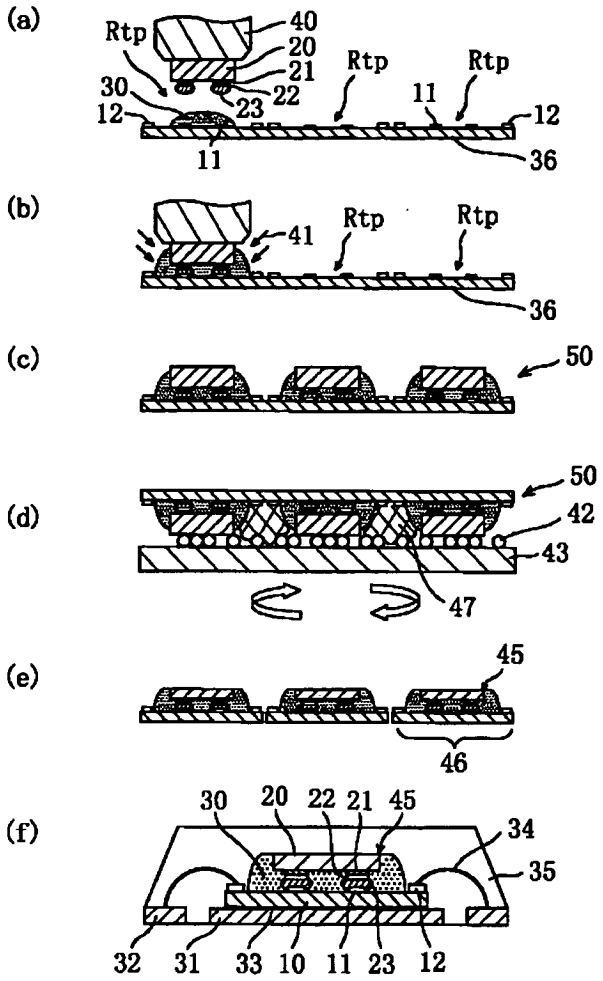
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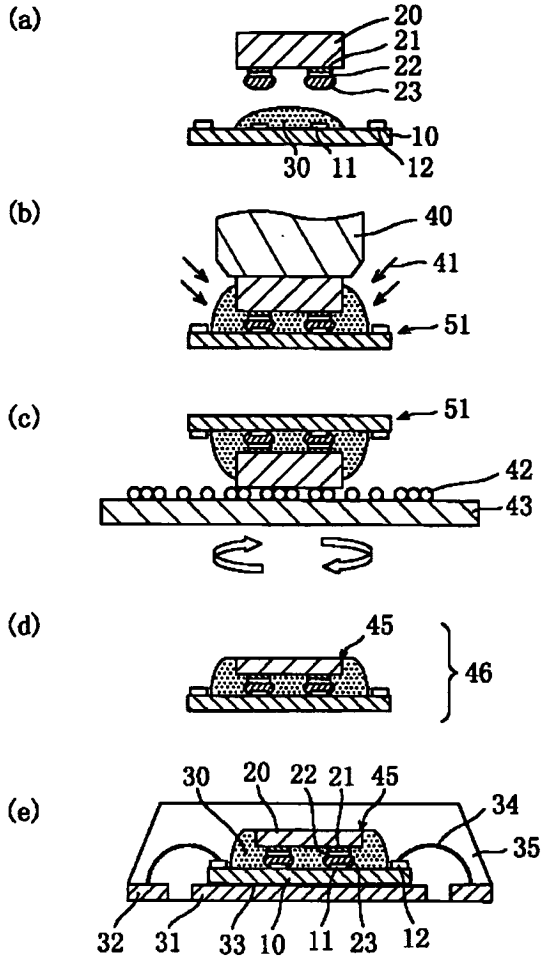
[Drawing 13]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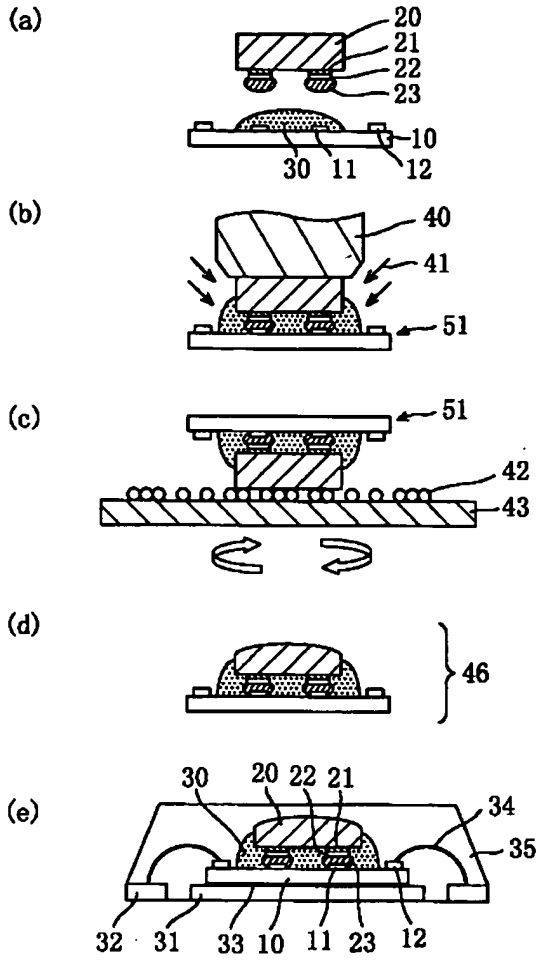
[Drawing 14]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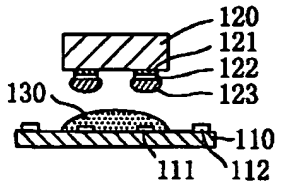
[Drawing 18]

(a)



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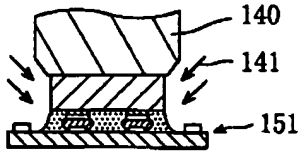

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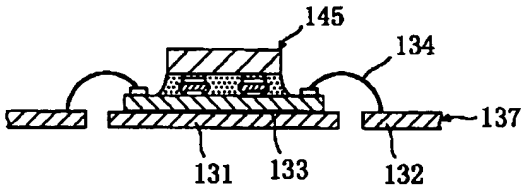

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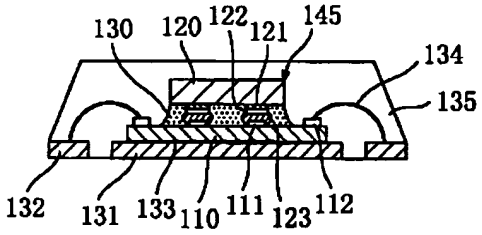

[Translation done.]